

# FPGA-based Visible Light Communication System for Real-Time File Transmission

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**Abstract** – The digital image, character/texts, audio (music), and video are the multimedia contents commonly used as objects to be transmitted on the VLC system. This paper has performed the real-time file transfer successfully using VLC technology with a UART connection. The FPGA was chosen as a DSP due to its capability in clocked-speed. We used an Ethernet connection due to its easy configuration and ability to meet the high-speed communication requirement. It was used for communicating between the host and the client device computer. This work covers the MAC layer implementation, SoC FPGA for UART connection, and analog front-end (AFE) transceiver. According to the functional test, the achieved bandwidth of the Ethernet connection is about 83.6 Mbps. However, the FPGA's clock is set at 100 kHz only due to the transferred file does not require a high speed. Thus, the physical layer baud rate is fixed to 11520 bps; it can be used for real-time transfer of a digital image with 512 pixels with no compressed file and error at 22 cm of optical LoS channel (no lenses).

**Keywords** – File transfer, FPGA, Real-time, Visible Light Communication

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## 1. Introduction

Visible light communication (VLC) is prevalent research and considered to be applied en masse in the future for an alternative communication system. This condition, along with the encouragement of research by various higher education approaches in the world and the start-up company focuses on the development of VLC technology [1]. Most of the VLC practices are sending multimedia content, such as simple character/text, audio, video, and digital images [2]. The data packet transmission is for internet broadcasting purposes or the delivery of human vital health data (e.g., EEG, ECG, EMG, etc.) [3].

S-M. Zhang et al. demonstrated the VLC system to run directly the audio stored in SD-card to the loudspeaker [4]. Later, R. Sagotra and R. Aggarwal carried out the image and audio transmission via visible light [5]. Later, K.S.S Raju et al. reported the PC-to-PC image and text transfer using low power LED [6]. Later, H. Kalla and M.V. Lakshmaiah developed optical wireless communication (OWC) system using the PWM technique to run a simple text from PC-PC via white LED [7].

However, we found that Ref. [4], [5], [6], [7] implement the VLC using microcontroller technology. Therefore, the clock speed is limited. To obtain higher throughput with low-latency, a proper DSP for the VLC system is mandatory.

H. Guo et al. proposed the field-programmable gate array (FPGA) as an option for high-speed VLC [8]. However, they did not implement it into a real VLC. We have also implemented a VLC technology for audio transmission systems [9], [10]. As in [9], [10], we do not use the DSP in the VLC transceiver blocks. Thus, there is a high possibility of data losses during the communication process.

For this reason, a real-time file transfer through visible light spectrum using an FPGA board is demonstrated by this paper, where the small-size content (digital image) is chosen as a transmitted object.

## 2. Methodology

### 2.1. System Specification

Before performing the file transmission using VLC, we need to design the VLC system first, as shown in Figure 1. System-on-Chip (SoC)-based FPGA configured the UART connection. In this work, we do not use any modulation.

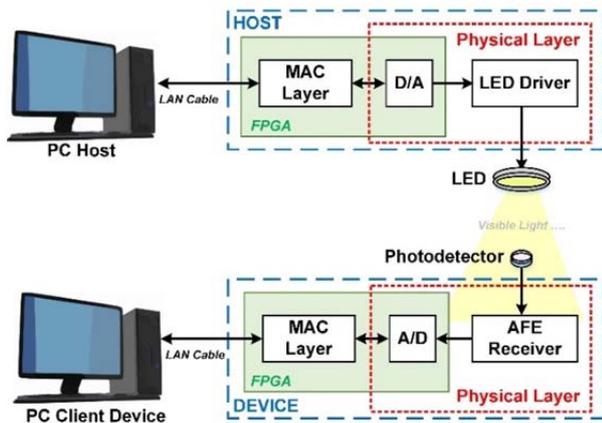


Figure 1. Overall block diagram of VLC system using FPGA for real-time file transfer

Our VLC system consists of the access point (host) and the client device (user). In outline, it is divided into two blocks, i.e., 1) Medium Access Control layer (MAC) that serves the communication path setting and the sent data packaging. Thus, it will enable directional- and bidirectional-communication, which

depends on the application. 2) Physical Layer (PHY) functioned to execute the sending and receiving data. The PHY layer consists of two parts, i.e., analog front-end (AFE) module as analog signal processing block, D/A to convert bitstreams into analog signals, and A/D to convert analog signals into bitstream signals. We used phosphor white LED as an antenna and photodiode as photo-sensor

### 2.2. MAC Layer and Network Design

MAC layer will be programmed on the FPGA; in this work, we used the ZYBO® board. The MAC layer is expected to do tasks as follow:

- 1) Deliver and receive the MAC frames from the host-to-device (H-t-D) or the device-to-host (D-t-H).
- 2) Perform IP packet MAC Frame's wrapping and unwrapping containing MAC trailer and header based on the VLC standard, which is IEEE 802.15.7.
- 3) Error detection. In this work, we used the CRC-16.

We designed the MAC layer in the form of a data frame containing three components as visualized in Figure 2, i.e., i) MHR; ii) MSDU; and MFR. Then, the frame control field is visualized in Figure 3. The wrapping process combines the data sent comprising MFR & MHR; meanwhile the unwrapping process performs the opposite.



Figure 2. The IEEE 802.15.7 MAC frame structure [11], containing frame control, sequence number, address information and security-related information, frame payload, and frame check sequence (FCS)

Frame Version	Sequence Number	Frame Type	Security Enabled	Frame Pending	Ack Request	Destination Addressing Mode	Source Addressing Mode
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Figure 3. The frame control structure of the IEEE 802.15.7 [11]

In this work, we used a point-to-point topology. The PHY layer's development is not complying with the standard, so the UART and Reed-Solomon will be used. Data exchanges between two nodes can be classified into two types: first is D-t-H, which is data exchanging mechanism between a personal computer (PC) and the ZYBO® board. The second one is the device-to-device (D-t-D) side, communication between the ZYBO® board and the ZYBO® board. Data exchanged is TCP/IP packet and done by using the Ethernet connection.

The Ethernet was chosen because the most popular wired internet connection is using a LAN cable. Furthermore, the ZYBO® board is equipped with Ethernet peripheral. Figure 4 depicts the block diagram of both the D-t-H and the D-t-D.

The SoC consists of two parts, i.e., hardware (H/W), which comprises used components, design architecture, and register settings. The register setting is applied to access H/W and software (S/W). The S/W counterpart consists of a Xilinx OS, MAC layer, and Reed-Solomon (RS). Figure 5 depicts the SoC design architecture for the H/W.

Zynq is a SOC that contains both an FPGA and ARM processor. In this work, we implemented our architecture in the ARM processor

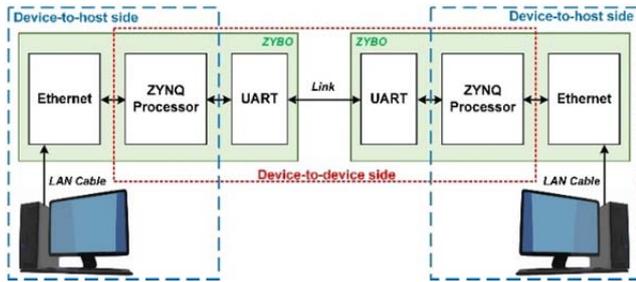


Figure 4. Complete diagram of data exchange mechanism

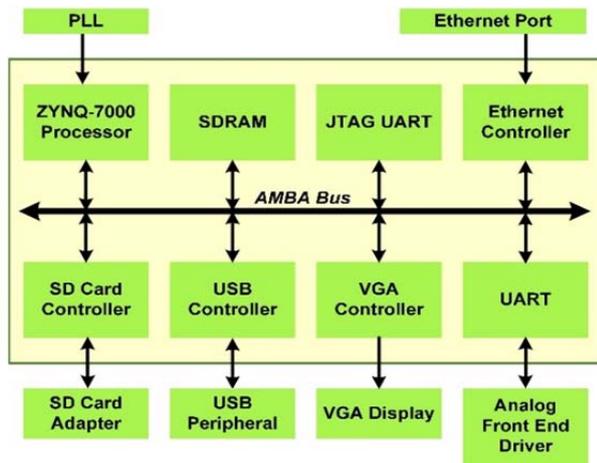


Figure 5. SoC Architecture design for real-time file transfer VLC

### 2.3. AFE Transceiver Design

The AFE transceiver (Tx-Rx) is shown in Figure 6. Since we directly connect the UART output to the LED driver, we used switch driver topology. To operate it, we have to control the transistor used from saturation to cut-off-condition (“1” to “0” or vice versa).

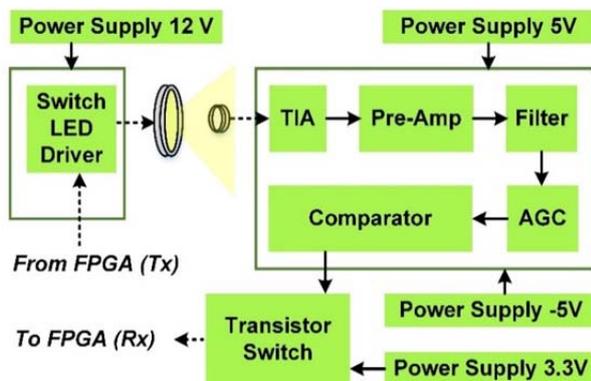


Figure 6. The diagram block of AFE transceiver

The 8 Watt of LED power was chosen from the CooChip® module (180° of viewing angle, 550 lumens, 12 V<sub>DC</sub>) produced by Hyrite Lighting. Co. The NPN transistor C1972 (V<sub>CC</sub> = 13.5 V<sub>DC</sub>, P<sub>O</sub> = 14

Watts,  $f = 175$  MHz,  $I_C = 3.5$  A) from Mitsubishi Semiconductors is selected.

Then, AFE Rx block consists of the following blocks:

- 1) Trans-impedance amplifier (TIA); this block has functioned to convert the photocurrent generated by the photodiode into the voltage ( $V_{TIA}$ ) [12].
- 2) Pre-amp configured as non-inverting to amplify the weak signal from TIA.
- 3) Analog filter; this block has functioned to reduce the optical noise.
- 4) Automatic gain controller (AGC); this block has functioned to compensate for the weak received signal when the AFE Rx module is changed against distance and angle [13].
- 5) Op-Amp comparator, this block has functioned to maintain the output signal in fully digital form. The comparator’s output has two values, i.e., high (5 V<sub>DC</sub>) and low (0 V<sub>DC</sub>) according to the determined threshold.
- 6) Transistor switch as the last stage, which acts to change the comparator's output voltage to fit the standard output voltage level of ZYBO® board, i.e., a 3.3 V<sub>DC</sub>.

We used all Op-Amps with TL072 from Texas Instruments, a general Op-Amp with has a cut-off frequency ( $f_c$ ) limits at 2 MHz; it is supplied by a dual power supply (5 V<sub>DC</sub>, ground, and -5 V<sub>DC</sub>). We selected BPW 34B photodiode ( $I_{sc} = 7.4$   $\mu$ A,  $\psi = 60^\circ$ ,  $\lambda = 350 - 1100$  nm,  $A_r = 7.45$  mm<sup>2</sup>). The higher LED’s lumen, the higher is received power of the photodiode [14], [15].

## 3. Results and Analysis

### 3.1. Implementation of MAC Layer and Network Layer

This section briefly summarizes the MAC layer and VLC network system testing results, where the details will be discussed in another report.

Firstly, we perform the MAC Layer to deliver and receive the frame/MAC packet from the H-t-D and D-t-H by PING test; and it is successfully done (Figure 7). In this test, the ping test implies that there is two-way communication (while the implemented VLC is one way only through downlink connection). Thus, we use a cable as an uplink connection. In further research, we will use infra-red as the uplink device.

Later, we test the functionality of the wrapping process IP packet and unwrapping MAC frame. It is also already carried out. Then we examine the error detection utilizes CRC-16. Summarily, the CRC-16 performs well as there is no error in sending and receiving a data packet from the D-t-H or vice versa.

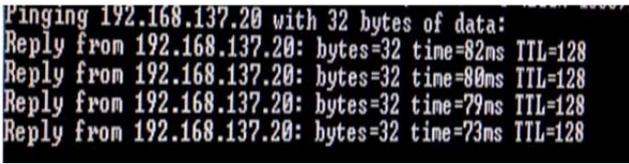


Figure 7. The Command prompt view

Afterward, we measure the Ethernet bandwidth using the *iPerf* tool, while the Python script is used to measure the UART bandwidth. We send serial data at a specific baud rate and achieved 83.6 Mbps average bandwidth and 921600 bps.

### 3.2. AFE Transceiver Implementation

Figure 8 depicts the hardware implementation AFE transmitter, and Figure 9 depicts the AFE receiver, which consists of TIA, Pre-amplifier, analog filter, and AGC. They are realized in each block for easy to use.

Figure 10 shows the digital oscilloscope (RIGOL DS1052E) display from the AFE transceiver's output. We use a signal generator signal (GW-INSTEK GDS-1152-AU) with a square form,  $f = 50$  kHz, as an LED driver input. Simultaneously, the LED transmits a signal and is received by the photodiode. The next block of AFE receiver processes the  $V_{TIA}$ .

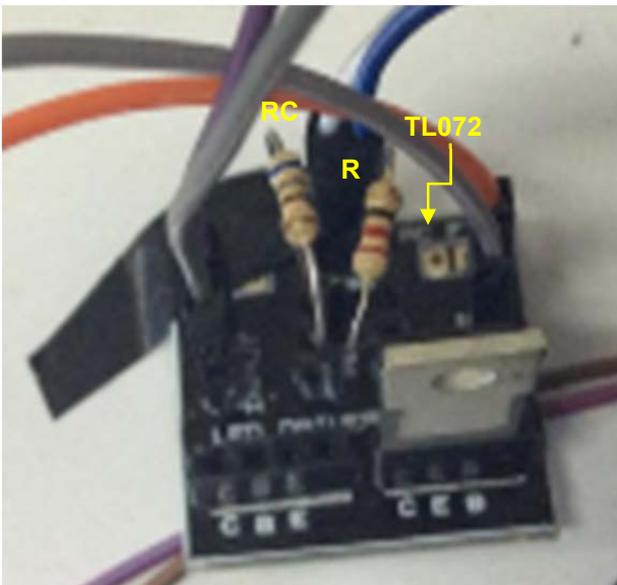


Figure 8. A Photograph of switch LED driver which consist of  $R_b$ ,  $R_c$ , LED socket, and single transistor MITSUBISHI C1972

One of our system's challenges is the AFE transceiver module; it limits at  $\sim 150$  kHz. The consideration in selecting components (i.e., Op-Amps and transistors) is not carried out to perform the light-based wireless file transfer. Therefore, we are only clocked as fast as 100 kHz in FPGA. We used 115200 bps instead, but this frequency does not make a flicker on the LED and can be used for image transmission.

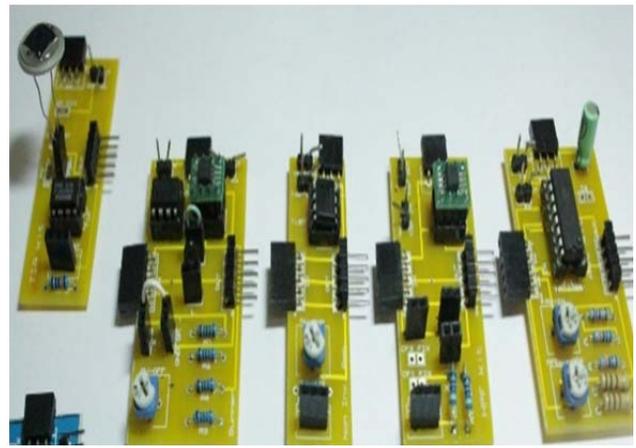


Figure 9. A Photograph of AFE receiver module fabricated in double layer printed-of-board (PCB), from left side to right side respectively are: TIA module, Pre-Amp, Analog Filter, and the last is AGC. The transistor switch is assembled in different module

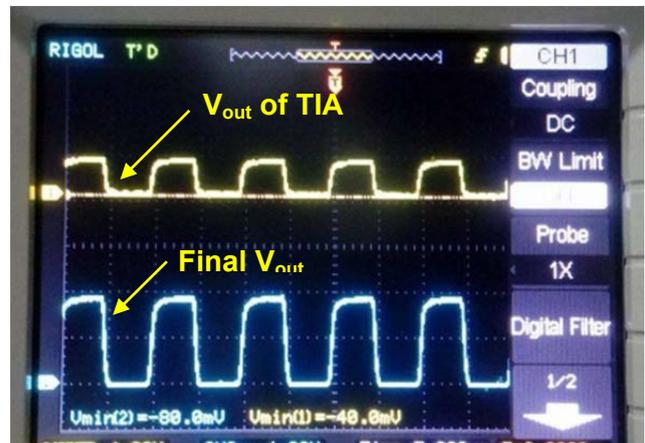


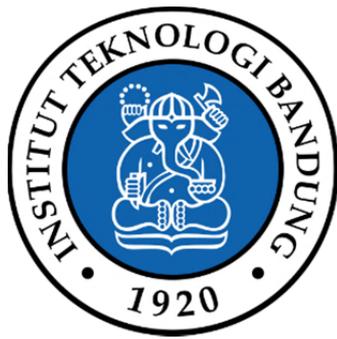
Figure 10. A Photograph of AFE transceiver, the output signal of TIA is indicated in yellow color and the output of transistor switch is indicated in blue color

### 3.3. System Demonstration

This work focuses on the functionality test according to the experimental set-up stated in Figure 1. Thus, the test is aimed at whether a file transfer via visible light capable of working well or not. It is done by connecting the client device to the PC using Ethernet wire. Meanwhile, the LED and the photodiode are faced perpendicularly (line-of-sight channel). We set the distance between transmitter and receiver to 22 cm with no optical lenses involved in the system.

Three PCs are used in this experiment; the first PC is to display the received image (PC-Rx 1), the second PC is to view the sent packets from the host (PC-Tx), and the third PC is to view the received packets by the client device (PC-Rx 2).

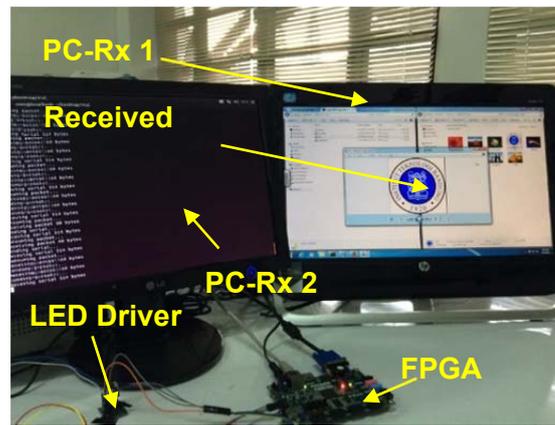
The system can smoothly stream the digital image (as shown in Figure 11) without image compresses, exactness, and no error. The correlation between BER against the SNR will be discussed in another paper.



(a)



(b)



(c)

Figure 11. A Photograph of experimental demonstration: (a) original image (.JPEG extension) with 512 pixels and 500 kb of file size to be transmitted; (b) transmitter side; (c) receiver side

#### 4. Conclusion

The real-time transfer of multimedia content (digital image) utilizing VLC using an FPGA board has been presented. We use a scenario point-to-point communication with a one-way link (downlink). Compared to Ref. [4], [5], [6], [7], [8], our VLC system offers a real-time system. Compared to Ref. [9], [10], our system enables a high-speed VLC system due to the use of the FPGA Xilinx Zynq-7000 board as the DSP.

In this paper, the PC-to-PC image transfer experiment is set only at 22 cm of the optical channel with a line-of-sight configuration. The distance which is too short is limited to the use of the photodiode (can generate maximum photocurrent only 7.4 $\mu$ A at 100 lux). In line with the demonstration, it can be shown that our work was successful with no flicker effect on the LED and no extraction of the received digital image. The MAC layer complies with the VLC worldwide standard, which is IEEE 802.15.7. The CRC-16 algorithm is implemented for error correction. Performance assessment shows that the Ethernet connection has 83.6 Mbps of bandwidth and ~921600 bps bandwidth of the PHY layer baud rate. Nonetheless, it is fixed to 115200 bps because the transferred file does not require an extremely high-speed like an HD quality video.

For the upcoming issue, we will be undertaking wireless internet access via VLC using our platform. Therefore, it is imperative to develop the MAC layer, which has a complete structure, e.g., dimming and multiuser support. Moreover, to increase the VLC system reliability, the RLL 8B10B and Manchester encoding are incorporated into our system. In the AFE block, the Op-Amps with a specific purpose need to be used. Thus, the larger-bandwidth will be achieved, and it will be capable of transmitting the data up to 1 Mbps of communication's speed.

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