

Improvement on LiFePO₄ Cell Balancing Algorithm

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Abstract – The paper presents improvement on operation time of cell balancing algorithm compared to conventional multiple cell LiFePO₄ charge methodology. A flowchart is synthesised to explain the main steps of the software design, which afterwards is implemented in a microcontroller. Experimental results are provided to clarify the transition between charge and balance process. Graphical data for a voltage equalization of eight cells is presented to verify the proposed improvement.

Keywords – Algorithm, Cell balancer, LiFePO₄, Switched shunt resistor topology.

1. Introduction

Improvement in the efficiency in today's transport is one of the key components in preservation of the environment. Electric vehicles (EV) are currently the available alternative but they have to offer reliability and better performance as well. Modern EV solutions include high energy density rechargeable lithium batteries, such as Li-Ion, Li-Po, LiFePO₄, etc [1]. Their structure, as a battery pack consisting of tens to thousands connected in series or/and parallel separate cells, determines more complex charge than lead-acid batteries, for example. The equalization process of the included cells in the battery pack is known as cell balancing [2, 3, 4].

Battery life has strong dependence on cell imbalance. If imbalance is persisting continuously, the overall capacity of the battery pack decreases with significantly higher rate during operation and therefore reduces the efficiency of the EV [5, 6, 7].

Figure 1 depicts cell balancing topologies divided into two main categories – active and passive [8, 9, 10].

The passive cell balancers are most widely spread, as they are reliable and cost effective solutions. To balance the cells they reduce energy from a charged cell through a dissipating resistor. The discharge is discontinued when the cell equals the lowest voltage in the pack or predefined reference. Several charge cycles are needed to finish the process. There are two passive cell balancing operation modes - fixed and switched shunt resistor [11].

The active branch of the cell balancing topologies are with better energy efficiency, however the overall complexity and cost are also higher [12]. Basically, those topologies use energy transfer from a cell with higher charge to another with lower inside the battery pack. The three main categories are based on capacitors, inductor/transformers and dc-dc converters [13, 14, 15].

The paper discusses improvement on the efficiency of the cell-balance process with passive switched shunt resistor topology.

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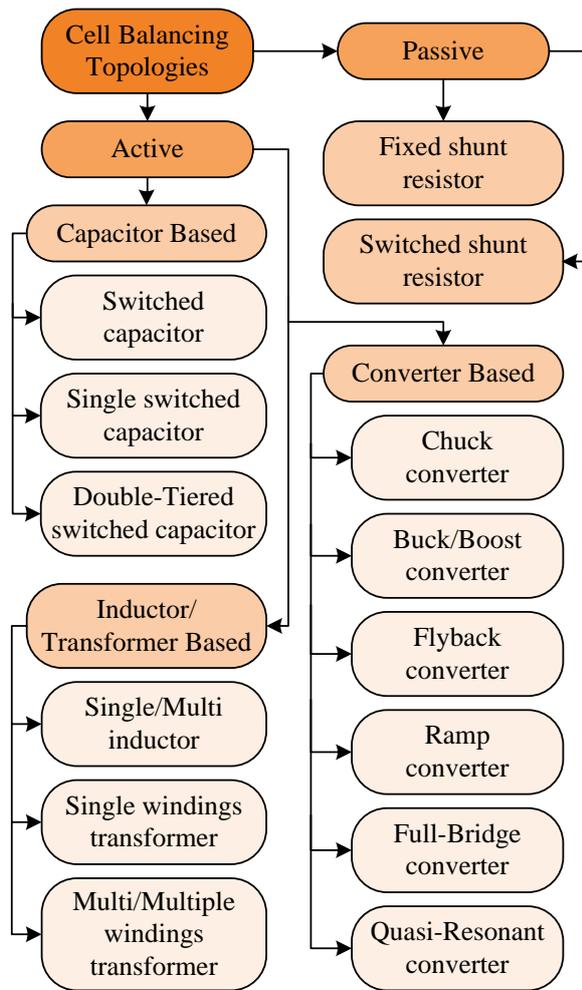


Figure 1. Cell-Balance topologies

2. Proposed cell balancing algorithm

The proposed improved cell balancing algorithm is presented in figure 2. After the initialization process of the microcontroller, several pre-measurement checks are accomplished. The main cycle starts with a delay of 100 ms. When permission is granted the 12 bit analog to digital converter (ADC) performs 1024 measurements of each cell voltage. A twelve multiplexed inputs are scanned in parallel, which is a significant improvement on overall rapidity of the system. After data acquisition finishes, the values are processed. This includes reduction of peaks (minimum and maximum) and the final values are averaged from the remained. Then a comparison with the predefined voltage cell balance values is done. The microcontroller decides whether to switch “on” or “off” the charging or cell balancing process.

The microcontroller monitors every cell of the battery pack for a preset overvoltage threshold, which is at $U_{\text{resh}}=3.65\text{V}$ for LiFePO_4 . When the first charge with nominal current $I_{\text{charge}}=10\text{A}$ has reached U_{resh} the improved balancing algorithm is triggered. The current through the dissipating resistor is $I_{\text{diss}}=0.4\text{A}$. After all cells in the battery pack decrease their voltage, to equal the cell/cells with lowest values, the discharge is discontinued. The second charge cycle defers from the conventional cell balance strategy (another charge with $I_{\text{charge}}=10\text{A}$). A reduction of 50 % of the nominal charge current to $I_{\text{charge}}=5\text{A}$ is proposed at this step. After another cells voltage equalization with the shunt resistors, the third reach of the threshold voltage reduces the charge current through the cells by another 50 % to $I_{\text{charge}}=2.5\text{A}$. Then the last equalization with a discharge is performed. The fourth charge cycle is performed continuously with charge current $I_{\text{charge}}=0.5\text{A}$ and a balance current $I_{\text{diss}}=0.4\text{A}$. This means that cells with higher charge receive only 0.1A flowing through them until all cells reach $U_{\text{resh}}=3.65\text{V}$. The proposed charge algorithm reduces the cell balancing time by 20 % compared to the conventional algorithm.

The improved algorithm is implemented in switched shunt resistor cell balancing topology. Figure 3 depicts the structure with “n” ($n=1, 2, 3,$ etc.) connected cells for a charge/balance.

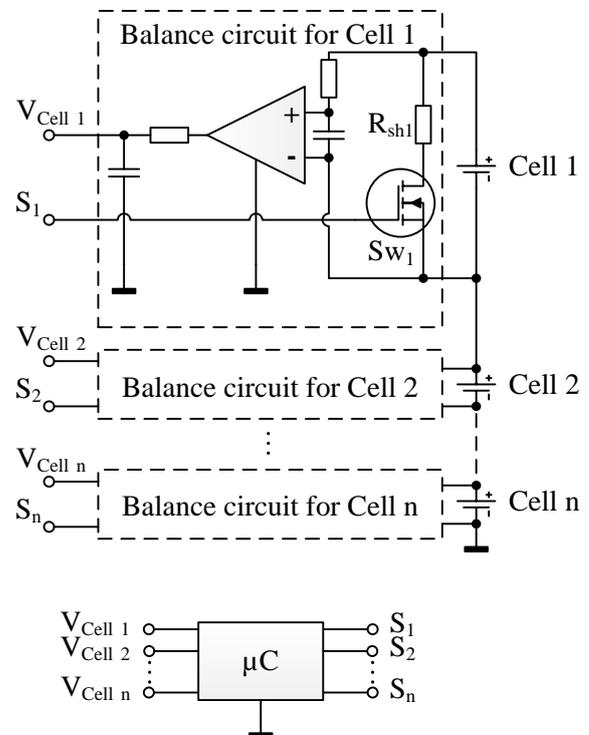


Figure 2. Cell-balancing circuit structure

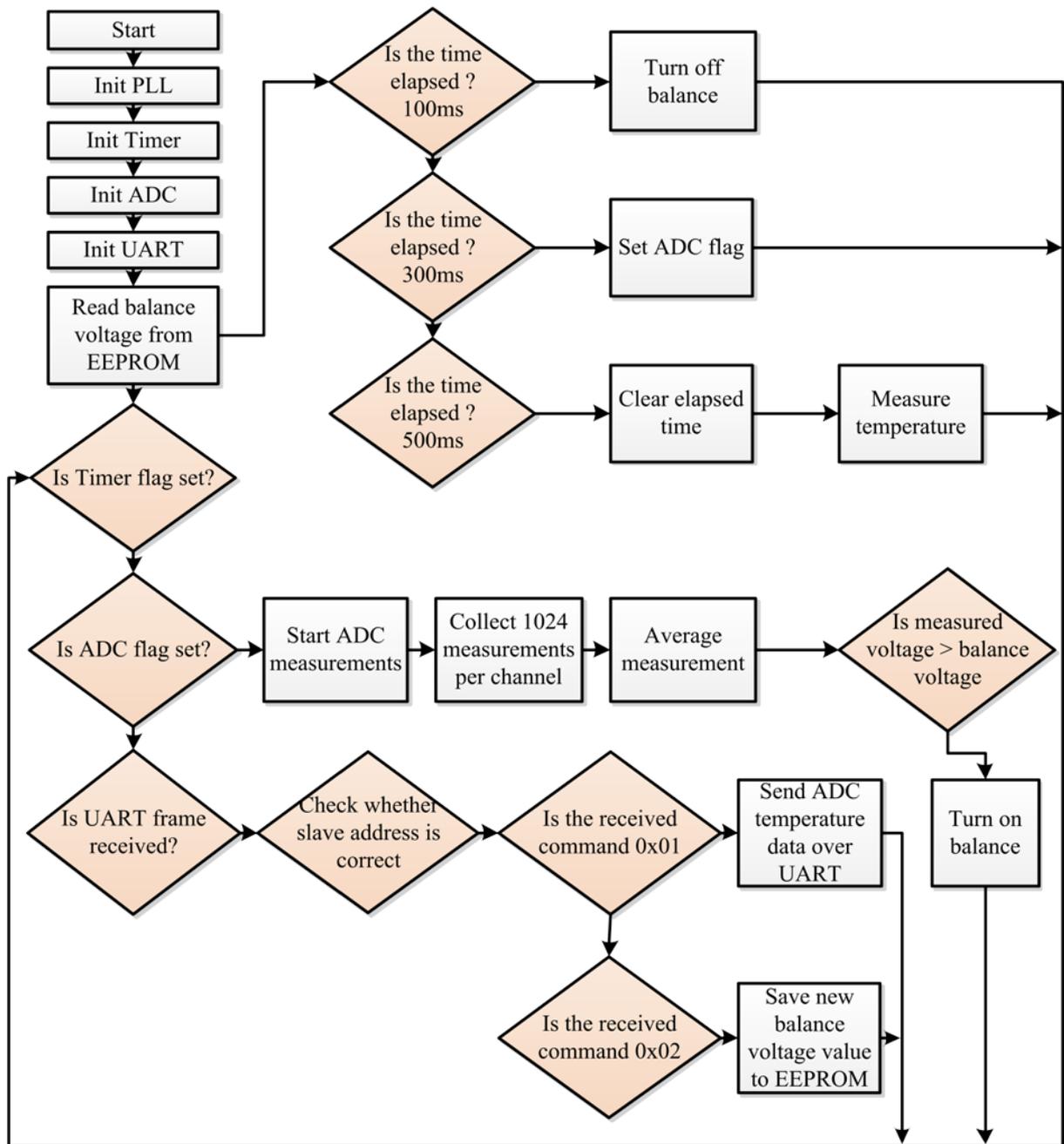


Figure 3. Proposed Improved Cell-Balancing Algorithm

Single balancer is consisting of a power electronic switch Sw_1 , shunt resistor R_{sh1} and voltage measurement circuitry, which gives analog voltage feedback ($V_{Cell1}, V_{Cell2} \dots V_{Celln}$) to the microcontroller. Then the control signal ($S_1, S_2 \dots S_n$) is fed to the gates of the MOSFET's to achieve either continuous or pulse width modulation charge of each individual cell. PWM allows the change in the cell charge current and therefore to apply the proposed improvement of the cell balancing process. The number of connected cells (n) is determined by the microcontrollers I/O ports.

3. Experimental results

To approve the methodology given above, a $LiFePO_4$ pack consisting of eight cells connected in series is tested. Figure 4 describes the transition from charge with nominal $I_{charge}=10A$ current to the next cycle charge current $I_{charge}=5A$. The transistor's PWM frequency is set at one kHz.

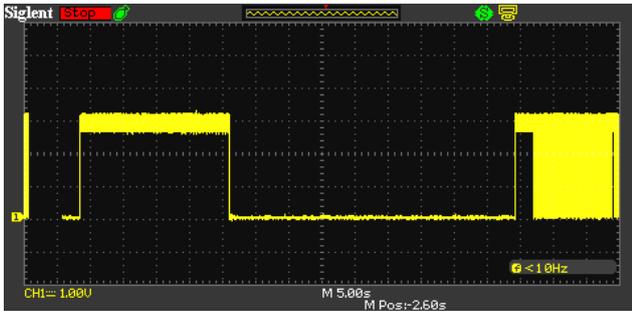


Figure 4. Change in cell charge current

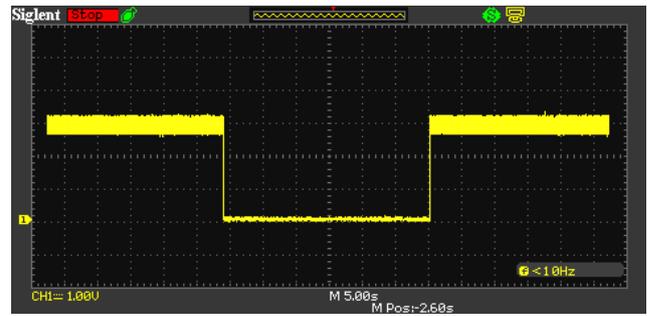


Figure 5. Thermal protection during operation

A thermal protection test is depicted in figure 5. The temperature measurement is done on a single point at every individual cell. The report is taken at every 500ms and the data is sent from every slave device (cell-balancer) to the microcontroller and then through RS485 transfer protocol to the battery management system, which decides whether to stop the charge/balance process. The temperature operating range is set at $0 \div 50^{\circ}C$.

Figure 5 depicts temperature rise above the allowed maximum and the interrupt in the charge process. The algorithm monitors the temperature and the charge/cell balance continues if the temperature returns within the temperature range.

Figure 6 depicts cell balance process of eight cells. Measurements of cell voltages are taken at every charge cycle. The time to charge the batteries with nominal charge current $I_{charge}=10A$ is not shown. On the graph are shown the following charge times:

- $I_{charge}=5.0A$ for 12 minutes;
- $I_{charge}=2.5A$ another 9 minutes;
- $I_{charge}=0.5A$ to finish the balance process takes 27 minutes.

Different colors describe different charge currents from uncharged/unbalanced in red to charged/balanced in green.

Table 1. Experimental results with eight cells

Measurement Point	Cell 1	Cell 2	Cell 3	Cell 4	Cell 5	Cell 6	Cell 7	Cell 8
0 min; I=5A	3,536	3,529	3,650	3,497	3,555	3,605	3,550	3,550
12 min; I=2,5A	3,633	3,593	3,650	3,571	3,643	3,648	3,641	3,634
21 min; I=0,5A	3,645	3,635	3,650	3,611	3,650	3,650	3,646	3,650
48 min; I=0,0A	3,630	3,630	3,630	3,630	3,630	3,630	3,630	3,630

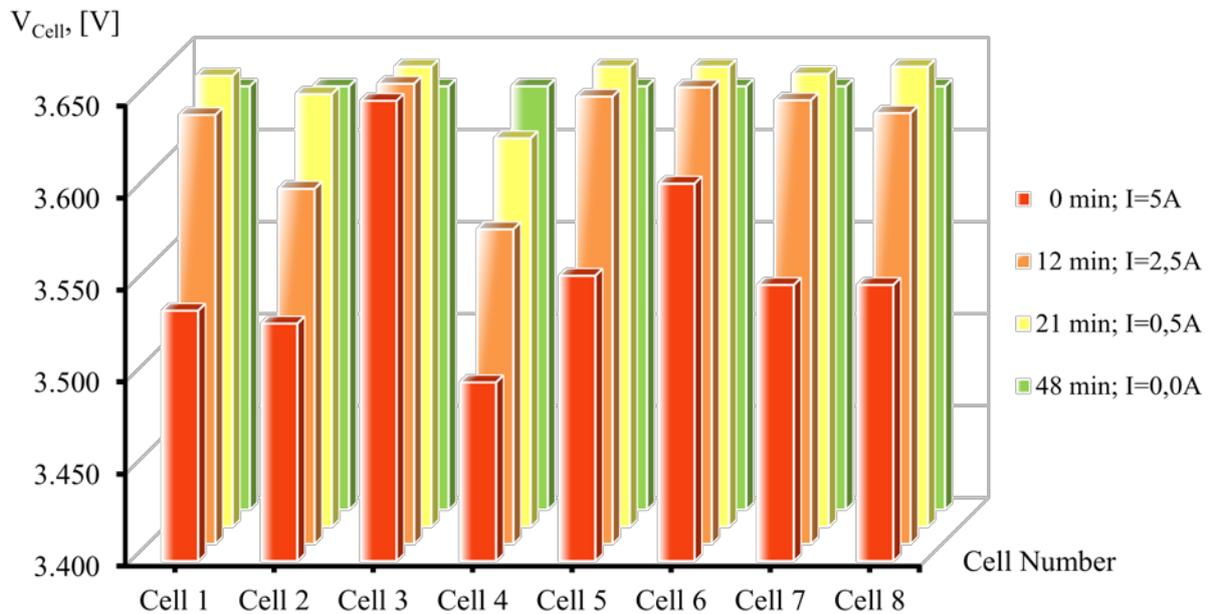


Figure 6. Cell-Balance process with the improved algorithm

Conclusion

The paper presents improvement of 20% on operation time of cell balancing algorithm compared to conventional multiple cell LiFePO₄ charge methodology with passive balance topology with switched shunt resistor.

A synthesis of a flowchart is done to explain the steps of the software design. The provided data measured with oscilloscope clarify the transition between charges of different current.

Graphical data for a voltage equalization of eight cells is then summarized to verify the proposed improvement.

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